

**Listing of Claims:**

Claim 1 (original) A non-volatile memory cell, comprising:

- a substrate, the substrate comprising a first region and a second region;
- a plurality of isolation structures positioned on the substrate, the isolation structures
- 5 comprising a first isolation structure positioned in the first region and a second isolation structure surrounding the second region;
- a control gate positioned on the first isolation structure in the first region;
- a first insulating layer positioned on the control gate;
- a second insulating layer positioned on the portion of the substrate in the second
- 10 region; and
- a floating gate positioned on the first insulating layer and the second insulating layer.

Claim 2 (original) The non-volatile memory cell of claim 1, wherein the portion of the floating gate positioned in the first region is stacked above the control gate.

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Claim 3 (original) The non-volatile memory cell of claim 1, wherein the floating gate comprises an opening positioned above the first insulating layer, and the opening is used to form a wire therein to connect to the control gate.

20 Claim 4 (original) The non-volatile memory cell of claim 1, wherein the substrate comprises a well of a first conductivity type positioned in the first region and the second region.

25 Claim 5 (original) The non-volatile memory cell of claim 1, wherein the substrate comprises at least a doping region of a second conductivity type positioned beneath the second insulating layer.

Claim 6 (original) The non-volatile memory cell of claim 1, wherein the isolation

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structures comprise field oxide layers or shallow trench isolation structures.

Claim 7 (original) The non-volatile memory cell of claim 1, wherein the first insulating  
layer comprises a composite layer composed of an oxide layer, a silicon nitride layer, and  
5 a silicon oxide layer.

Claim 8 (original) The non-volatile memory cell of claim 1, wherein the second insulating  
layer comprises a tunneling oxide layer.

10 Claims 9-20 (cancelled)